

AMENDMENT TO THE DRAWINGS

Please amend FIG. 6 as attached, wherein the gate insulating film 39 is depicted to have first and second insulating films 19 and 29, which is fully supported by the specification.

A marked-up version of Fig. 6 as well as a replacement Fig. 6 are enclosed in this response.

REMARKS

Claims 1, 2, 5-7, 9, 11-14, and 17-31 remain in the application.

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Final Office Action dated April 6, 2004 has been received and its contents carefully reviewed.

Applicant thanks the Examiner for allowing claims 5, 6, and 17-31.

In the Office Action, claims 1, 7, and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,137,551 to Jeong. Claims 7 and 10-16 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,672,888 to Nakamura. Claims 7 and 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Applicant's Related Art Figs. 1 and 2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong in view of U.S. Patent 5,920,362 to Lee.

Applicant cancels claims 3, 4, 10, 15, and 16. Applicant amends claims 1, 7 and 14 to recite more clearly the features of the invention that were inherent in the previously presented claims. Applicant submits that the claims as amended overcome the 112, second paragraph, rejection, and Applicant respectfully requests the Examiner to withdraw the rejection.

The rejections of claims 1, 2, 7, 9, and 11-14 are respectfully traversed and reconsideration is requested. Claim 1 is allowable over the cited references in that each of these claims recites a combination of elements including, for example, "a storage electrode buried in the gate insulating film to overlap with the gate line; and a protective layer on the gate insulating film to cover the data line, the gate line and the thin film transistor, wherein the pixel electrode is connected to the storage electrode via a contact hole passing through the gate insulating film and the protective layer." Claim 7 is allowable over the cited references in that each of these claims recites a combination of elements including, for example, "the storage electrode is connected to a transparent electrode pattern via a first contact hole passing through the second gate insulating

film and the protective layer and wherein the storage electrode includes the storage electrode and the gate line opposed to each other and having the first gate insulating film formed therebetween.”

None of the cited references, including Jeong, Nakamura, Lee, or Applicant’s Related Art, singly or in combination, teaches or suggests at least these features recited in the claims. Jeong discusses that “[t]he gate electrode 53G and the gate line 53L are formed on gate insulating layer 52” (Jeong, column 5, lines 33-35). In Jeong, the gate insulating film 52 is not “entirely covering” gate line 53L as recited in claim 1. Therefore, Jeong does not disclose or suggest at least this feature of claim 1.

In Figs 4(a) through 4(c) of Nakamura, “[t]he thin-film transistor has a glass substrate 201, a third gate electrode 202, a first gate electrode 203, a first gate insulating film 204, source and drain regions 205, a drain electrode 205b, an offset region 206, an active layer 207, a second gate insulating film 208, a second gate electrode 209, a first interlayer insulating film 210, a fourth gate electrode 211, a second interlayer insulating film 212, data lines 215, 215', gate lines 216, 216', a first contact hole 217, a second contact hole 218, a third contact hole 219, a first storage capacitance electrode 220, a second storage capacitance electrode 221, a third storage capacitance electrode 222, and a transparent pixel electrode 223” (Nakamura, column 6, lines 56-66). Fig 4(a) clearly shows electrode 221 above the surface of the gate insulating film 204 (Nakamura, Figs. 4(a)-4(c)). Nakamura does not disclose or suggest “the storage electrode is connected to a transparent electrode pattern via a first contact hole passing through the second gate insulating film and the protective layer and wherein the storage electrode includes the storage electrode and the gate line opposed to each other and having the first gate insulating film formed therebetween” as recited in claim 7.

Applicant’s Related Art in Figures 2 and 3C through 3E similarly shows the electrode 6 above the surface of the gate insulating film 9 (Applicant’s Related Art, Figs 2, and 3C-3E). Therefore, Applicant’s Related Art does not disclose or suggest “the storage electrode is connected to a transparent electrode pattern via a first contact hole passing through the second gate insulating film and the protective layer and wherein the storage electrode includes the storage electrode and the gate line opposed to each other and having the first gate insulating film formed therebetween” as recited in claim 7.

The Examiner does not allege that Lee teaches, discloses or suggests all of the features of independent claims 1 or 7, and in fact Lee does not teach, disclose, or suggest all of these features.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Accordingly, Applicant respectfully submits that claims 1 and 7, and 2, and claims 9 and 11-14 which depend from claims 1 and 7, respectively, are allowable over the cited references.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: July 6, 2004

Respectfully submitted,

By 

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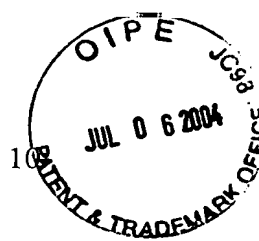
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Application No.: 10/028,300



Docket No.: 8733.508.00-US

The Examiner does not allege that Lee teaches, discloses or suggests all of the features of independent claims 1 or 7, and in fact Lee does not teach, disclose, or suggest all of these features.

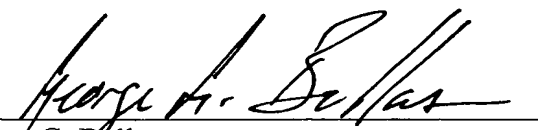
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MARKED-UP VERSION



FIG. 6

